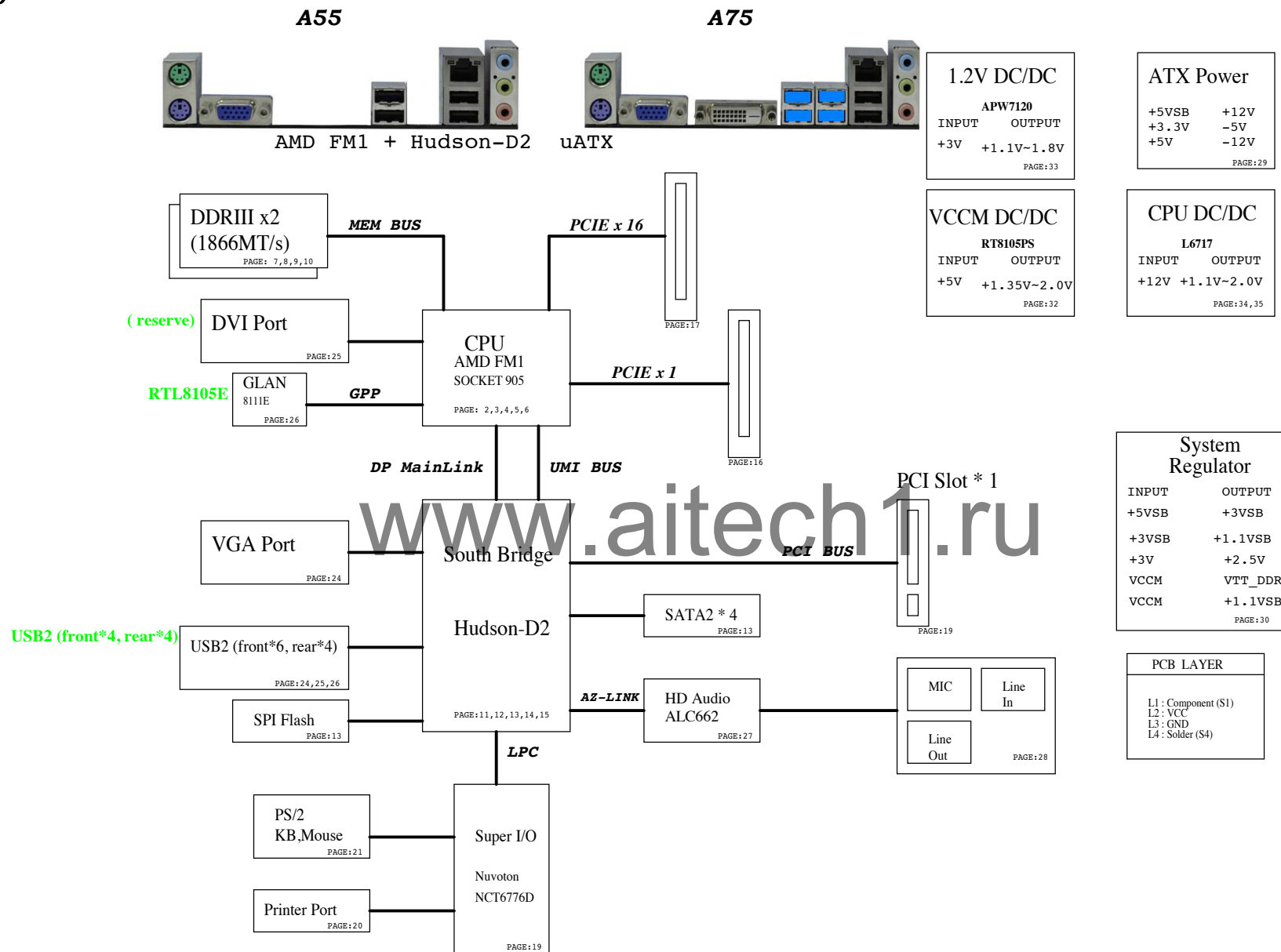


# A55M-VS

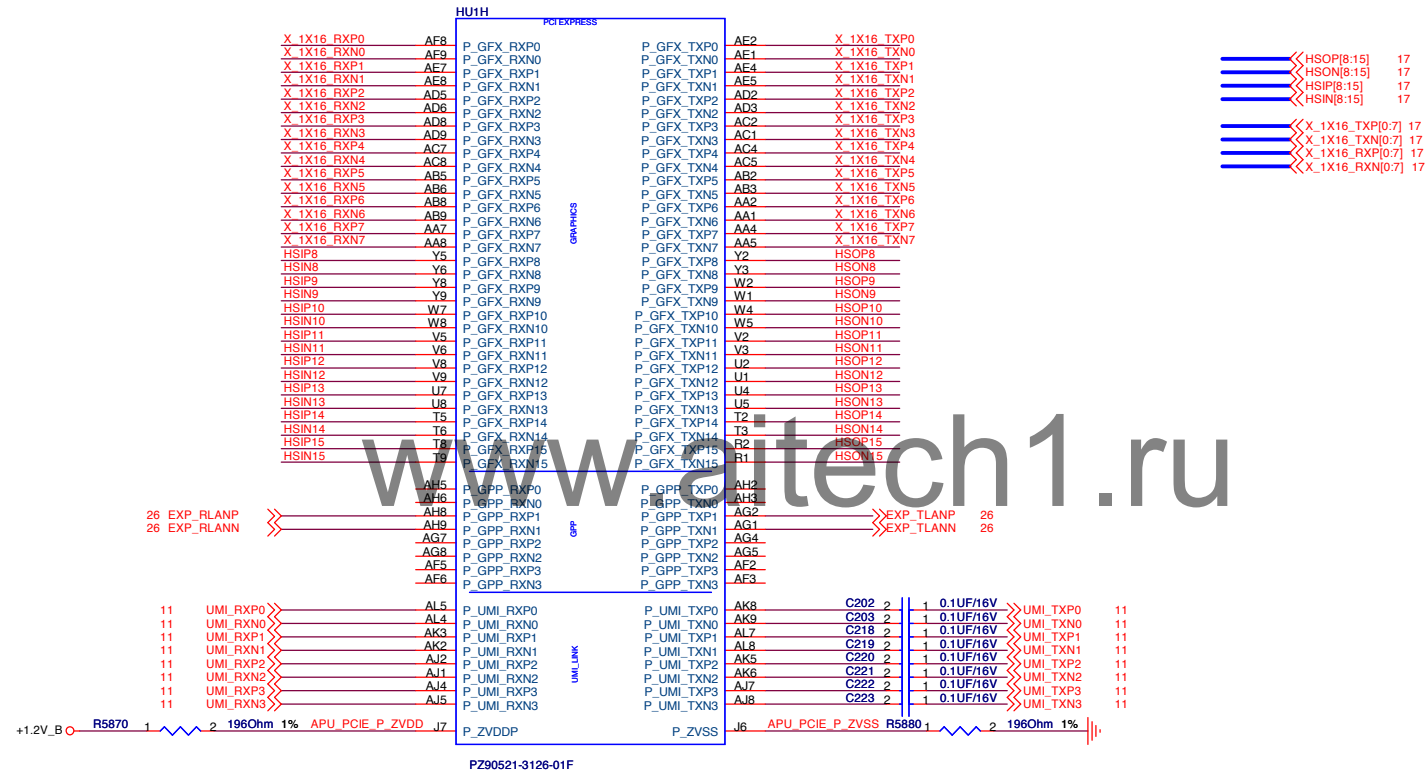
R.G/A 1.00



**CAD Note:**  
Default Resistor and Capacitor footprint is SMD 0402 type. Different resistor footprints are showed on schematics.

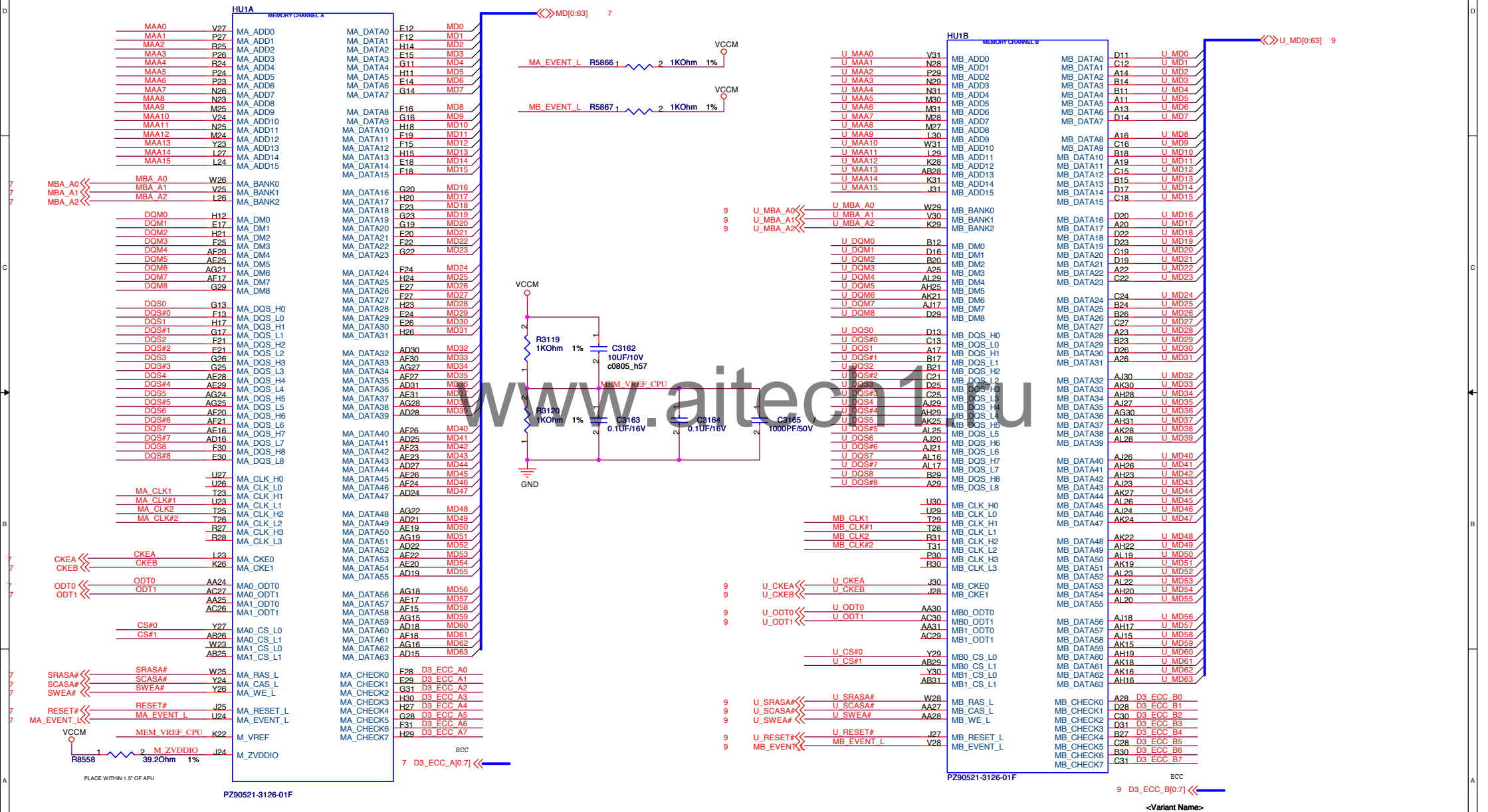
/ = Not Installed Part

## CPU HyperTransport Interface

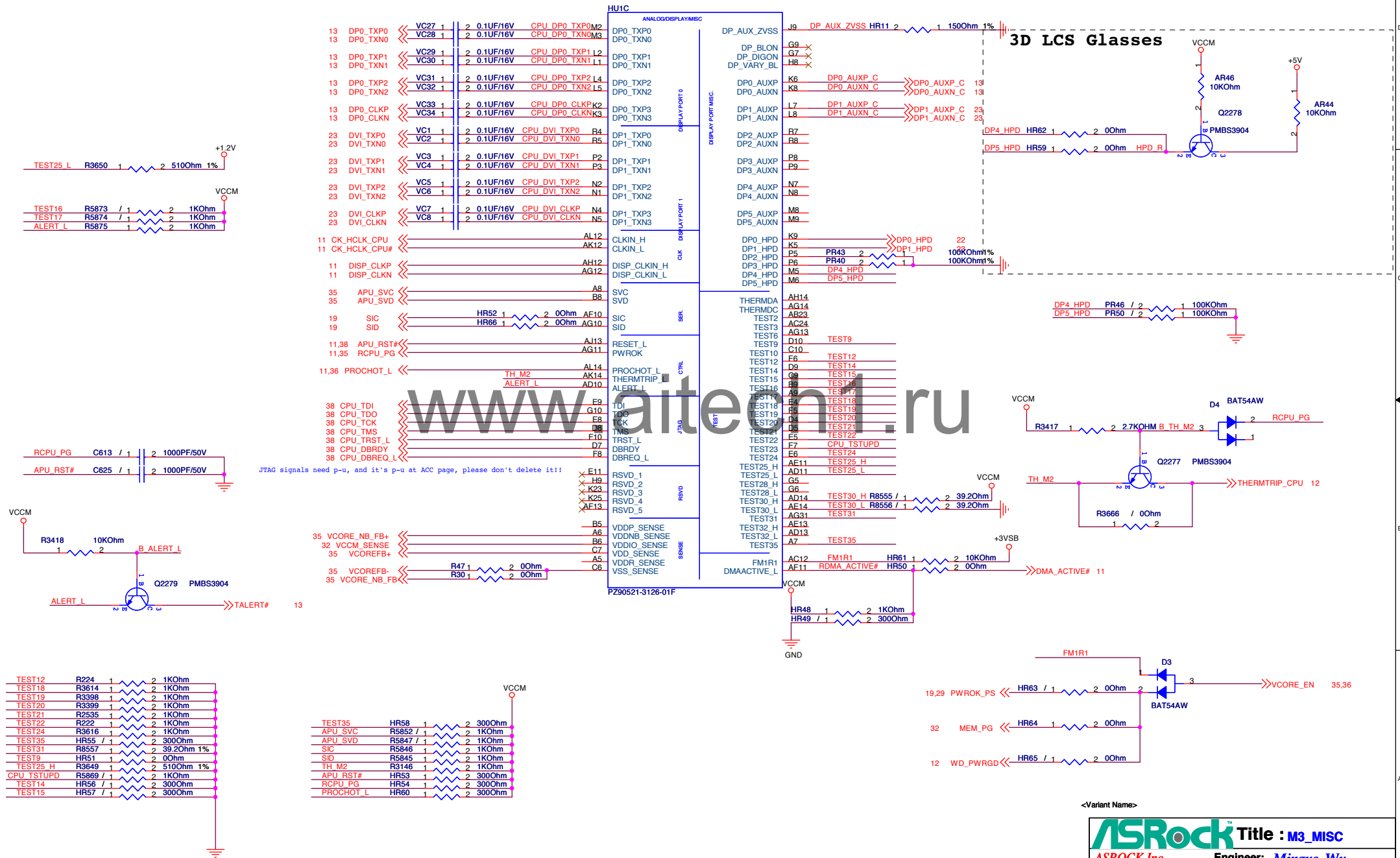


**<Variant Name>**

# CPU DDR3 Memory Interface

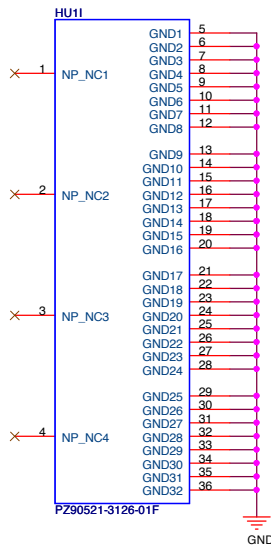
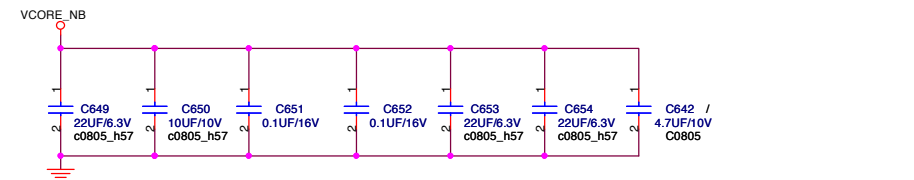
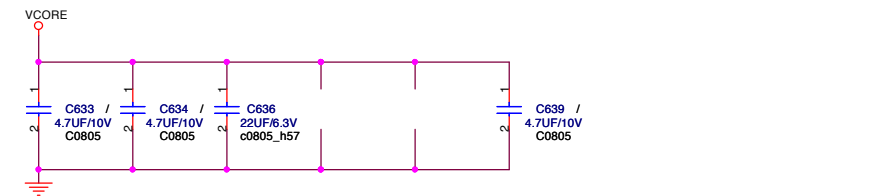
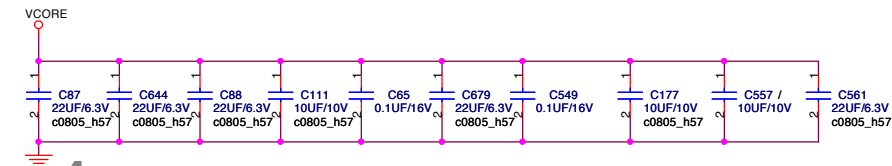
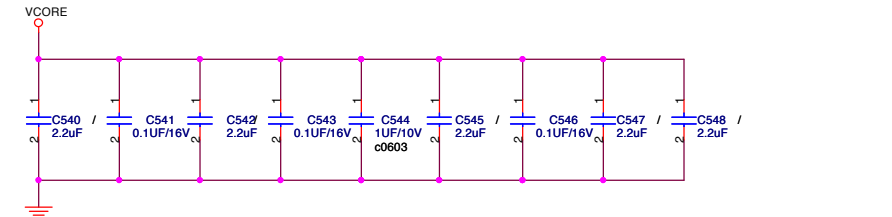
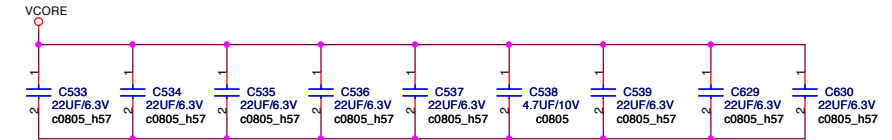
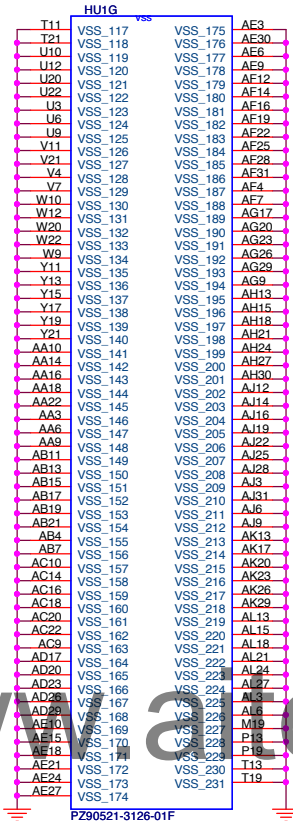
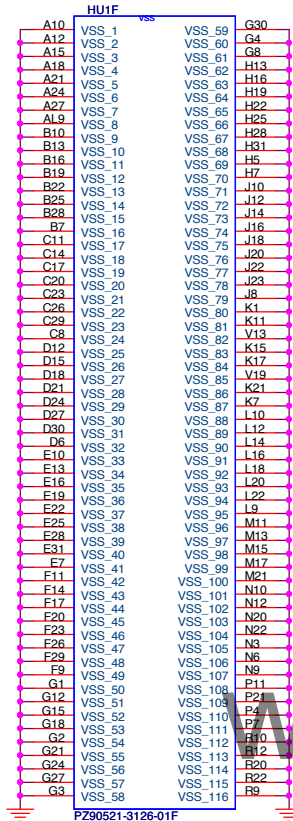
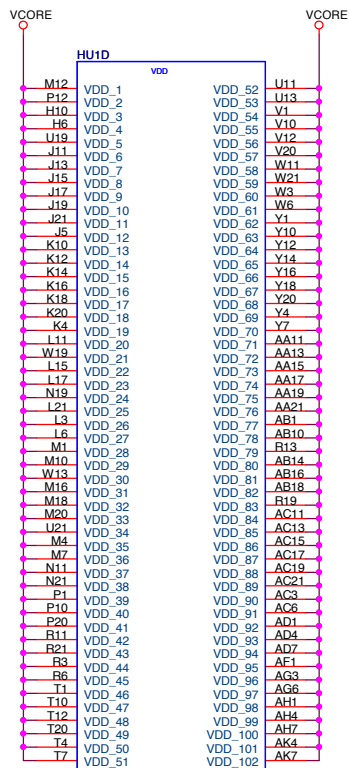


## CPU Control & Debug Interfaces

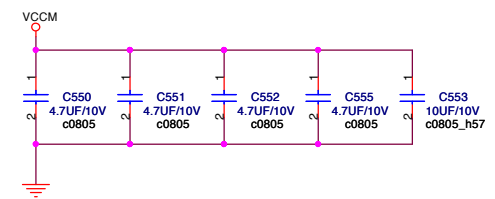
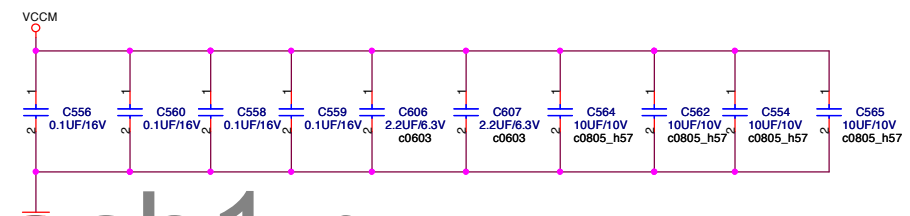
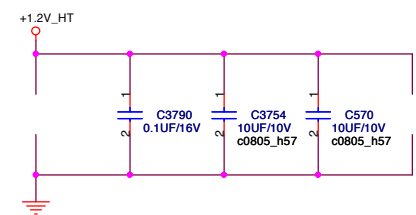
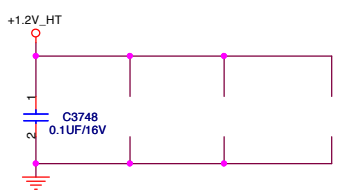
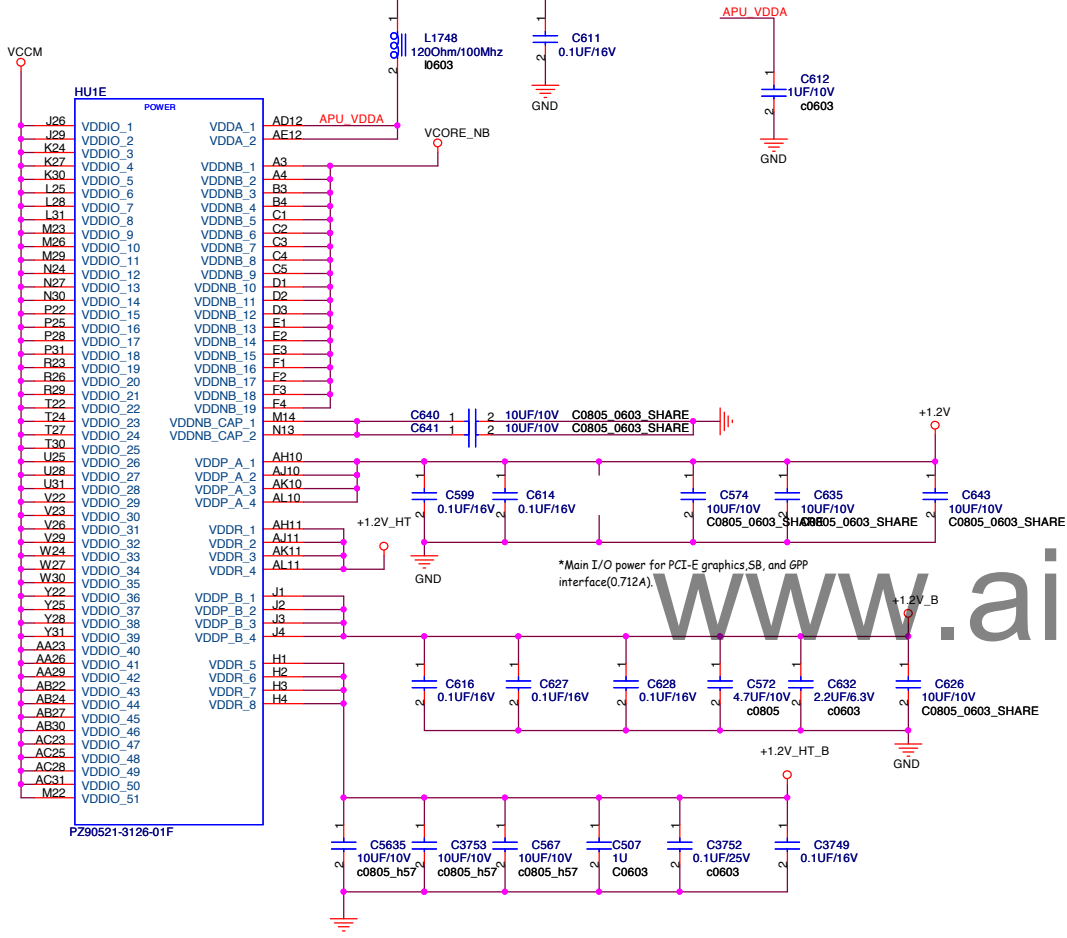


**<Variant Name>**

# Processor Power & Ground

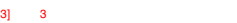


<Variant Name>



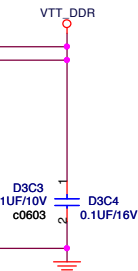
<Variant Name>

DDR3\_A1A A0



9 DDRSAPU <<\_\_\_\_\_

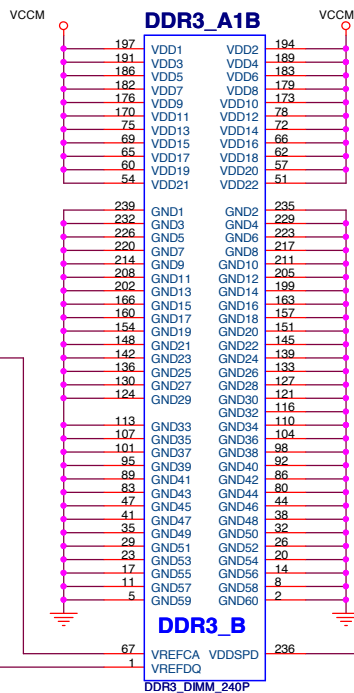
9 DDRSAPD <<\_\_\_\_\_



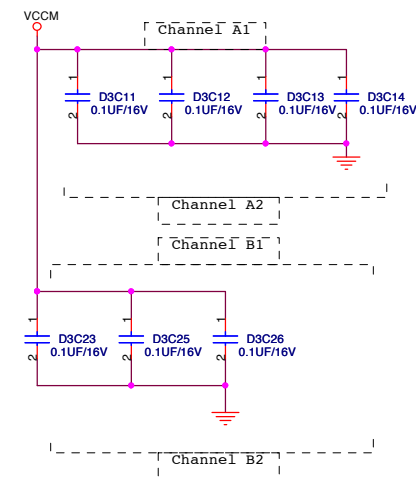
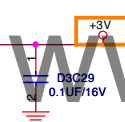
		<b>Title :</b> DDRIII_DIMM1&3	
<b>ASROCK Inc.</b>		<b>Engineer:</b> <i>Mingus Wu</i>	
<b>Size</b> A3	<b>Project Name</b>  <div style="font-size: 1.5em; font-weight: bold; color: blue;">A55M-HVS</div>	<b>Rev</b> 1.03	
<b>Date:</b> Monday, April 02, 2012		<b>Sheet</b> 7	<b>of</b> 39

10 D3\_VREFDQ  
10 D3\_VREFCA

If you don't use  
MEM\_WARN, please  
connect PIN116 and  
PIN 239 to GND.



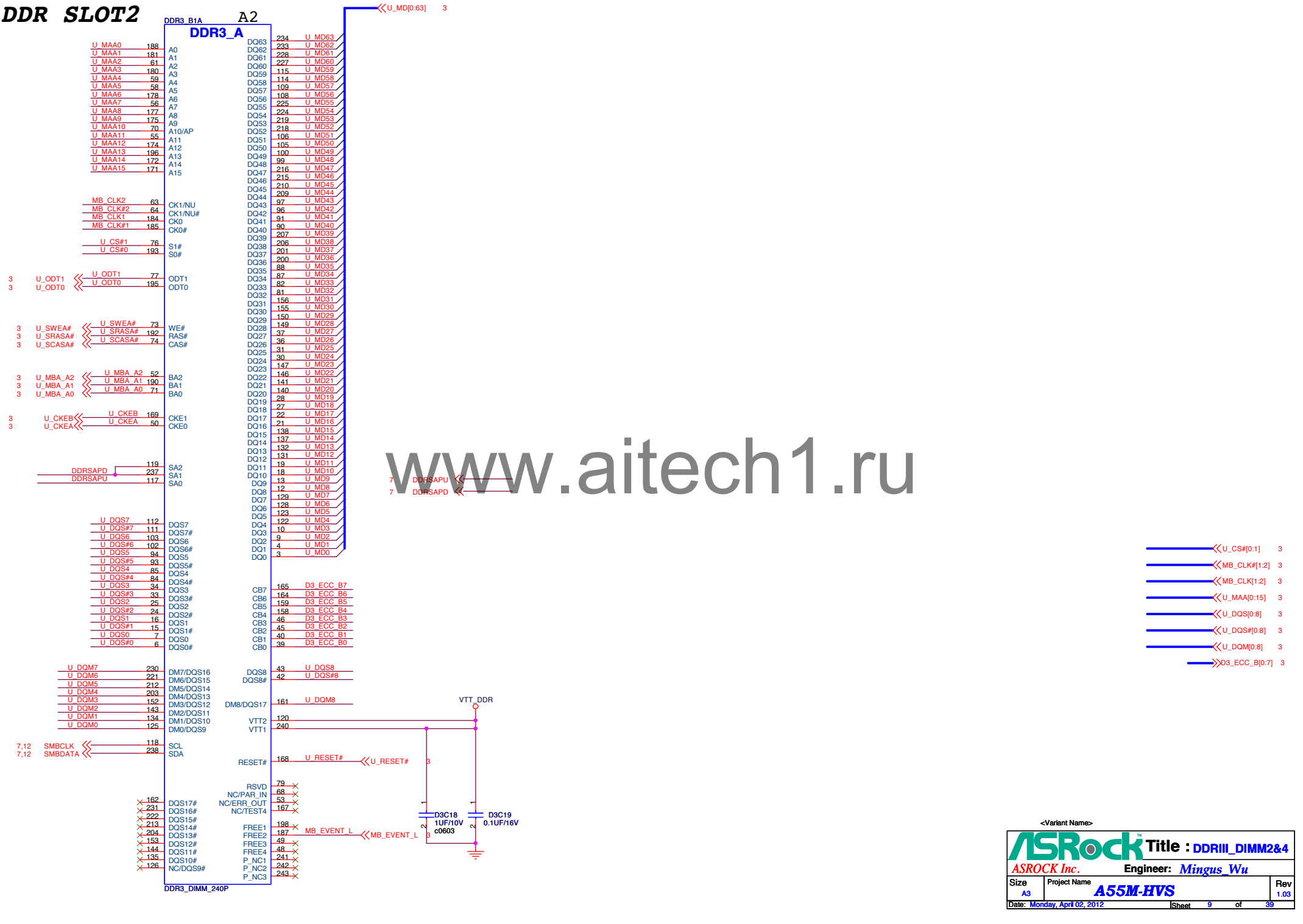
If you don't use  
MEM\_WARN, please  
connect PIN2 and  
PIN121 to GND.



With AMT    W/O AMT  
+3V\_CL    +3V  
S0-S5有電    S0有電

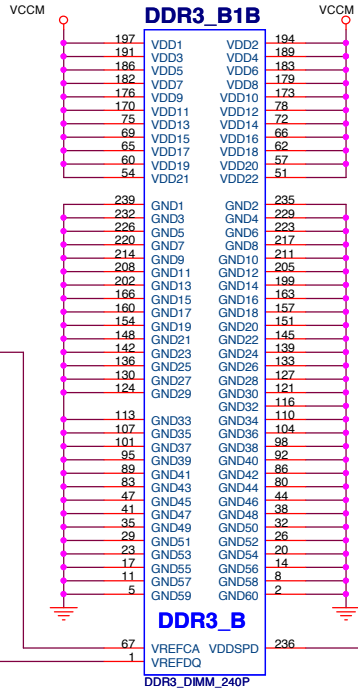
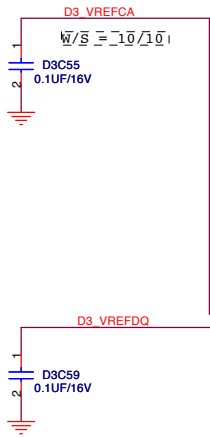
<Variant Name>

DDR SLOT2



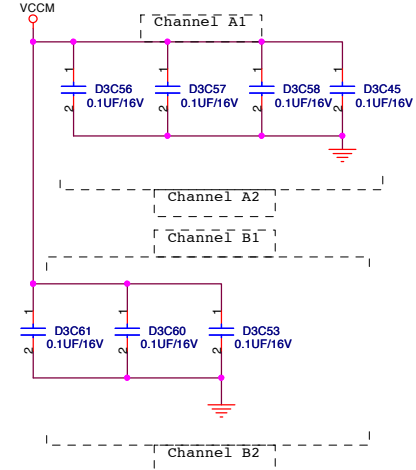
8 D3\_VREFDQ  
8 D3\_VREFCA

If you don't use  
MEM\_WARN, please  
connect PIN116 and  
PIN 239 to GND.



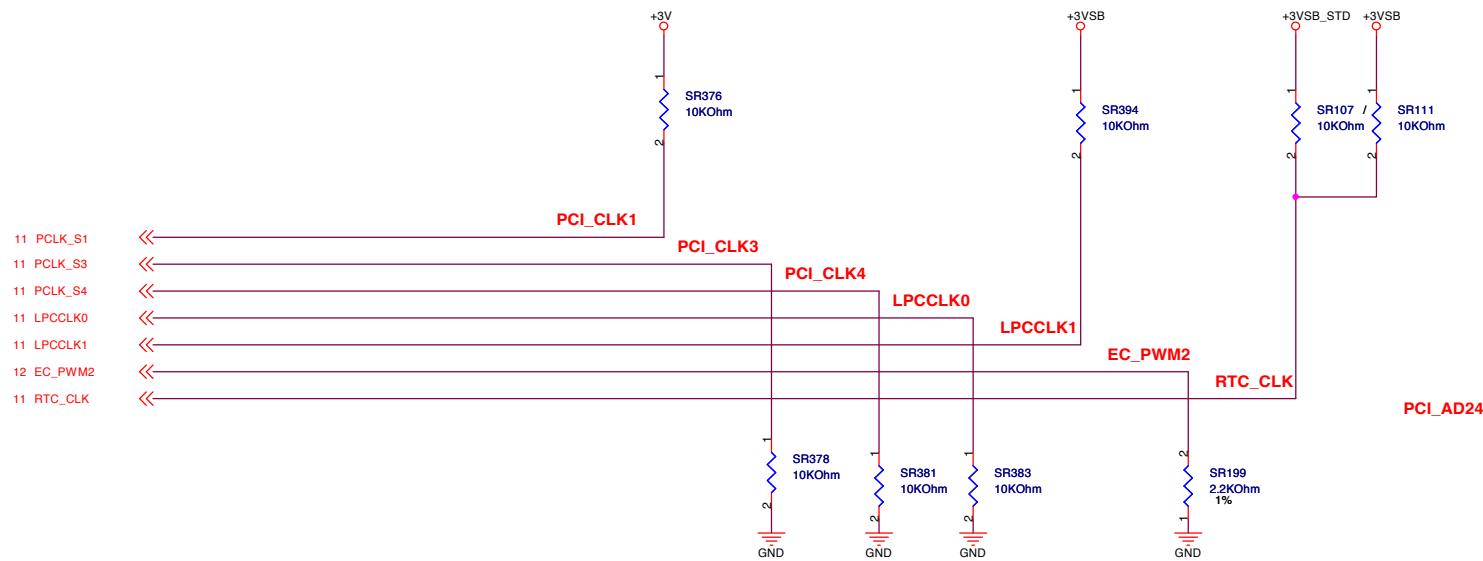
If you don't use  
MEM\_WARN, please  
connect PIN2 and  
PIN121 to GND.

www.aitech1.ru



With AMT W/O AMT  
+3V\_CL +3V  
S0-S5有電 S0有電

<Variant Name>



www.aitech1.ru


REQUIRED STRAPS

	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPCCLK0	LPCCLK1	RTC_CLK	EC_PWM2	PCI_AD24
PULL HIGH	Allow PCIe Gen2 DEFAULT	Enabled Debug straps	NON-FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	S5+ DISABLE DEFAULT	ROM TYPE: H = LPC ROM	Default PCIe straps
PULL LOW	Force PCIe Gen1	Disabled Debug straps DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	S5+ ENABLE	L = SPI ROM DEFAULT	EEPROM PCIe straps DEFAULT

<Variant Name>

www.aitech1.ru

<Variant Name>

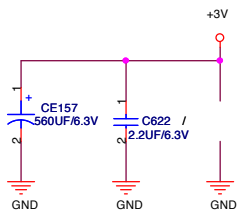
		Title : PCIE_X1 SLOT	
ASROCK Inc.		Engineer: <i>Mingus_Wu</i>	
Size A3	Project Name <b>A55M-HVS</b>	Rev 1.03	
Date: <i>Monday, April 02, 2012</i>		Sheet	16 of 39



White

A schematic diagram showing a capacitor labeled C58 with a value of 0.1UF/16V. The capacitor is connected between a -12V supply and a ground symbol.

No any crystal:11MHz/3V

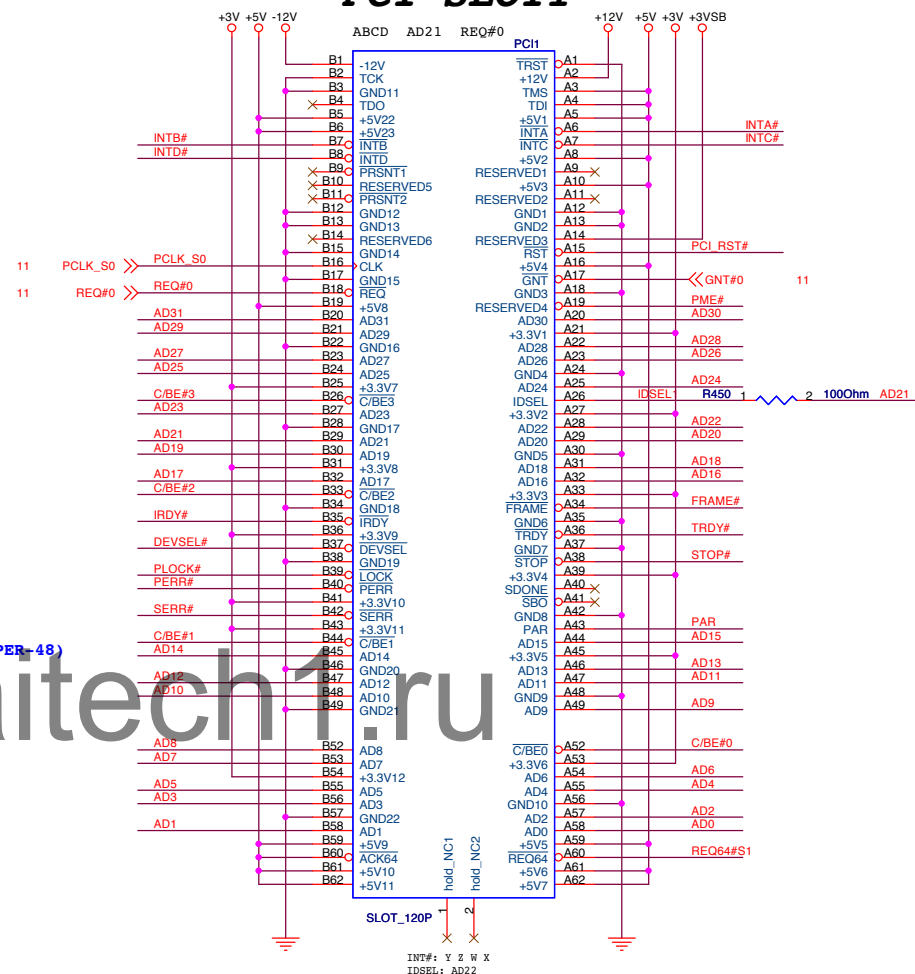
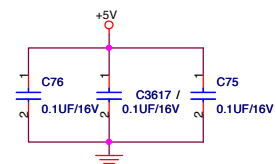
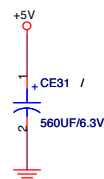
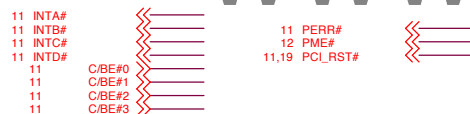
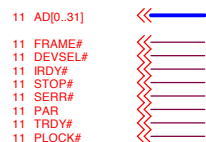


P1.0 and p1.1 are open drain pin

flash method:

- ## 1. ICP

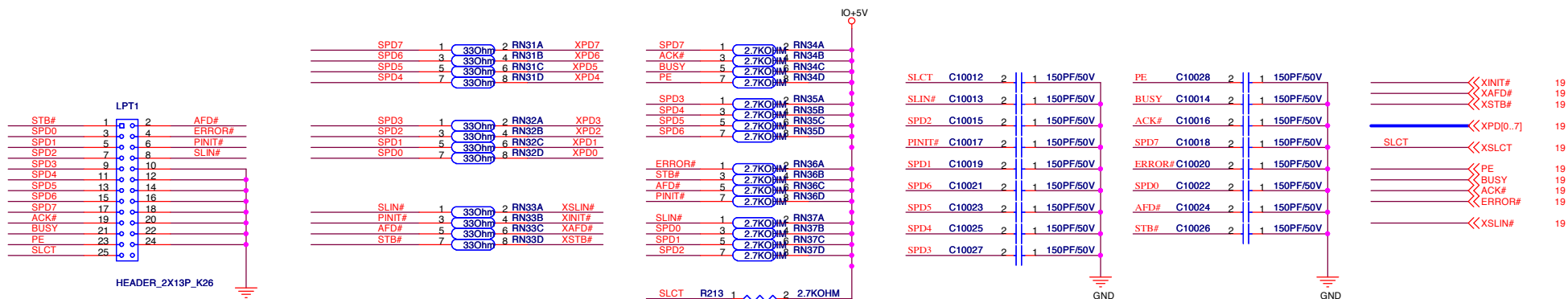
```
2.writer(Advantech---labtool-48UXP, LEAP--LEAPER-48)
```



<Variant Name>



## Parallel Port

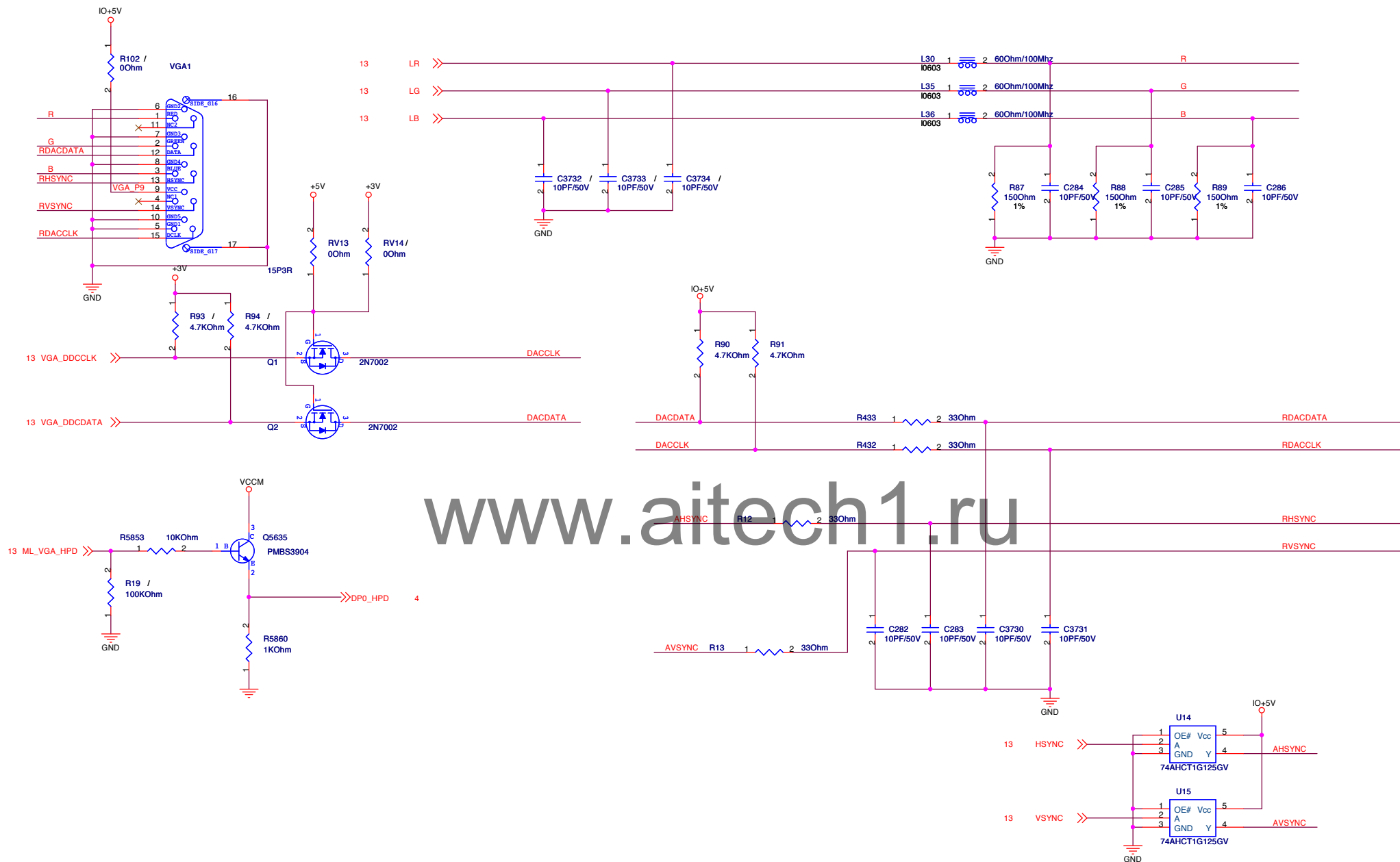


[www.aitech1.ru](http://www.aitech1.ru)

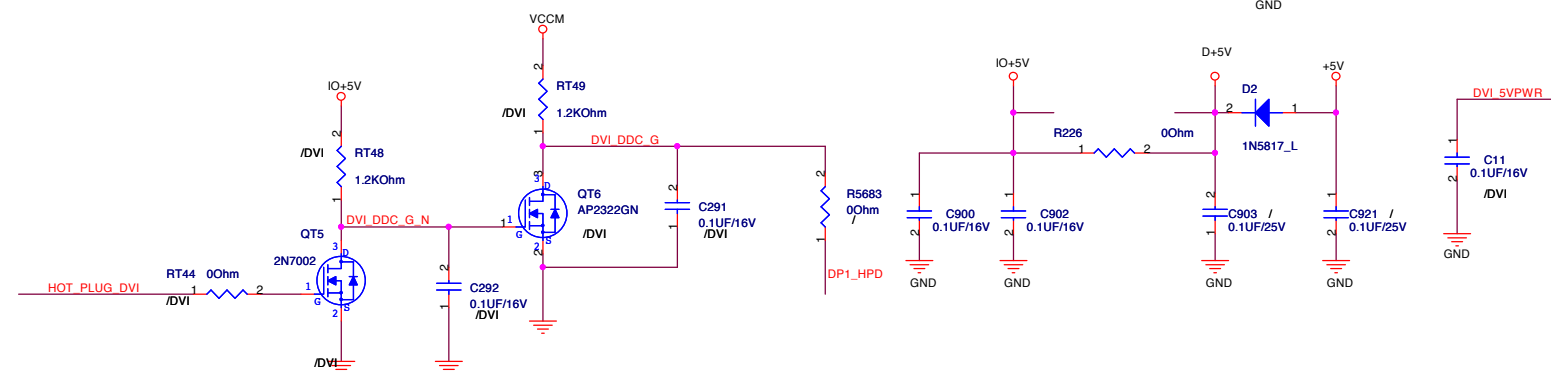
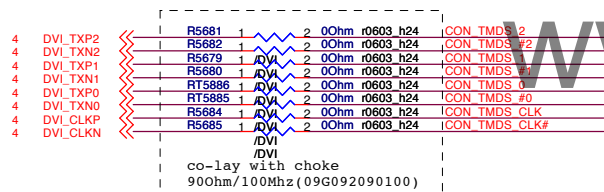
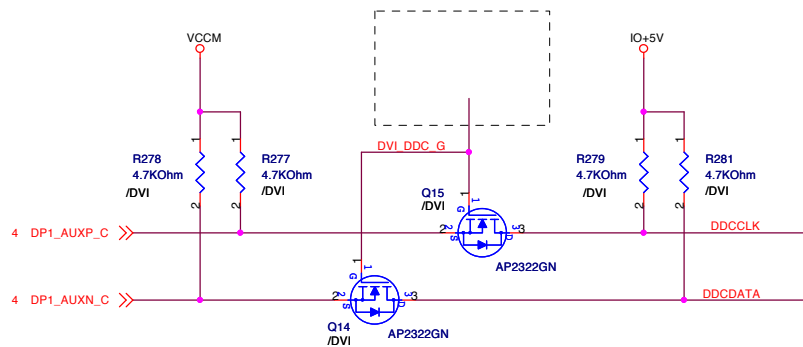
**<Variant Name>**



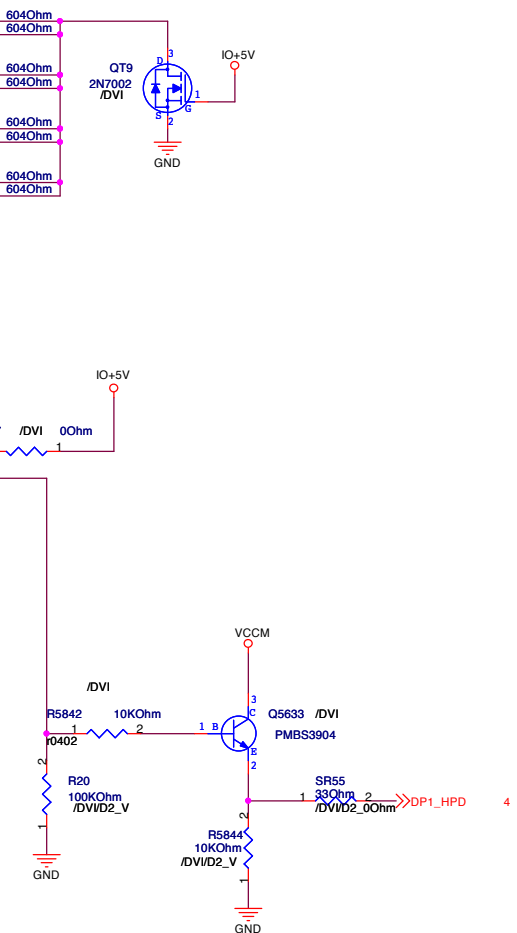
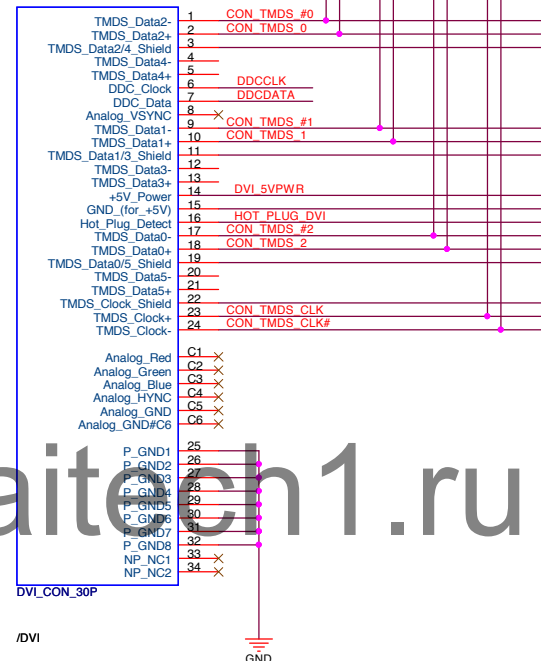
www.aitech1.ru

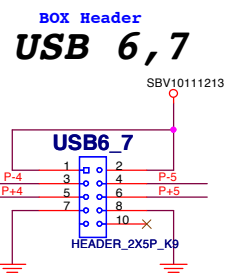
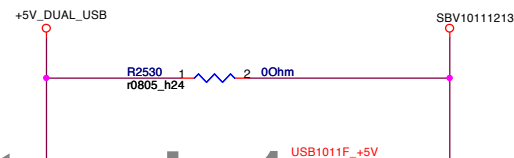
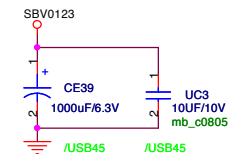
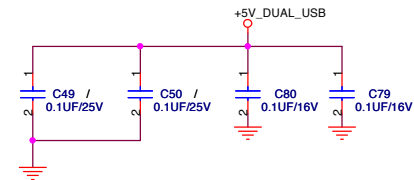
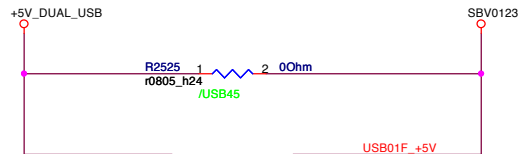


<Variant Name>

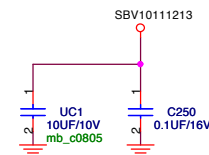
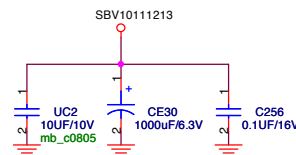
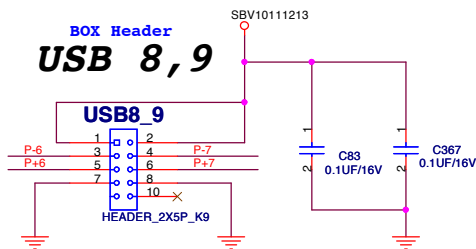


# DVI1





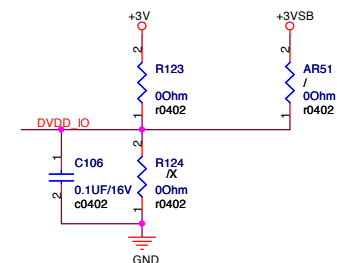
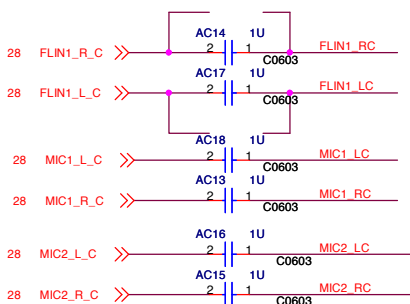
**BOX Header**



<Variant Name>







NOTE: ASUS symbol mistake  
Pin45: SIDE L  
Pin46: SIDE R

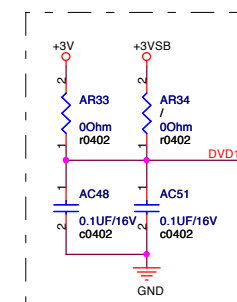
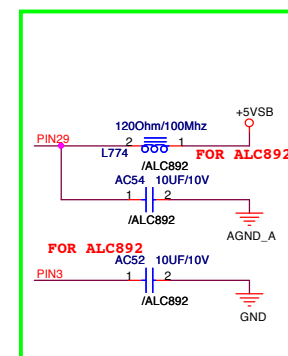
2009/05/06  
Update form Mars

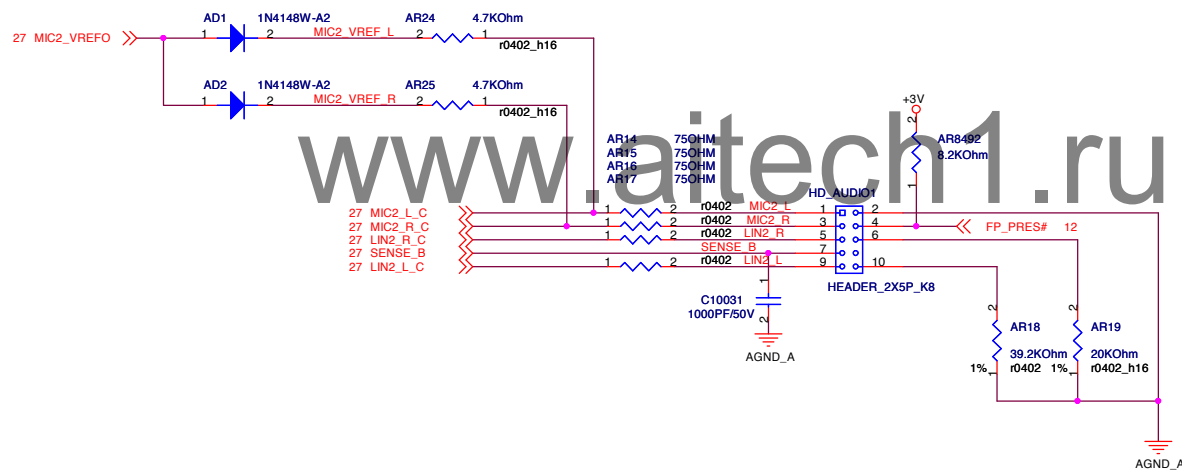
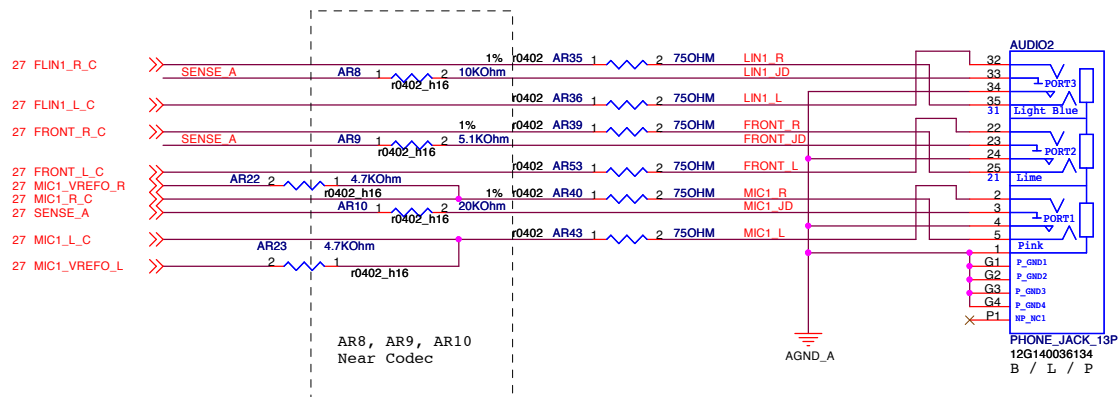
2009/05/06  
Update form Mars

Place one near codec and another one near external connectors.

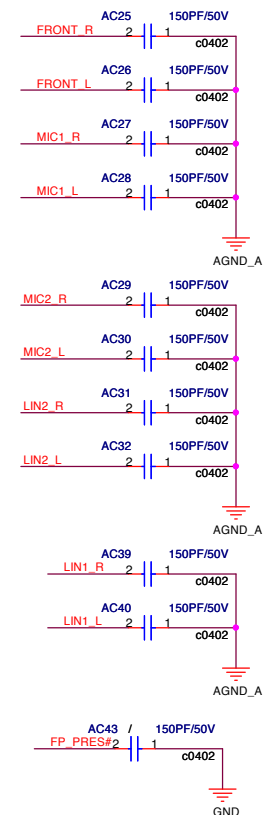
ASUS  
ASROCK

<Variant Name>



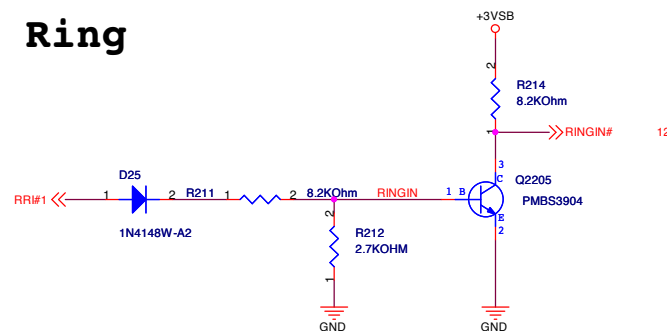


For EMI

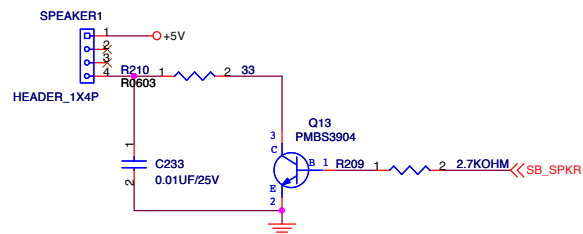


<Variant Name>

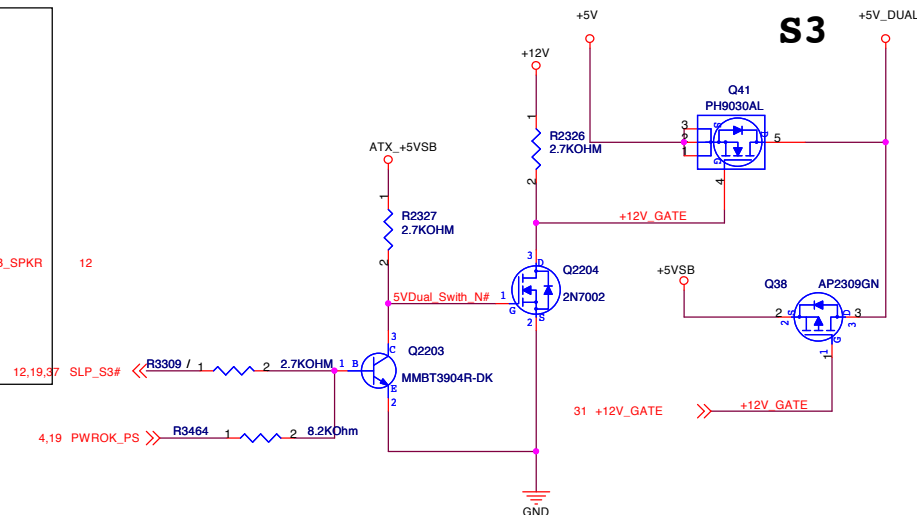
# Ring



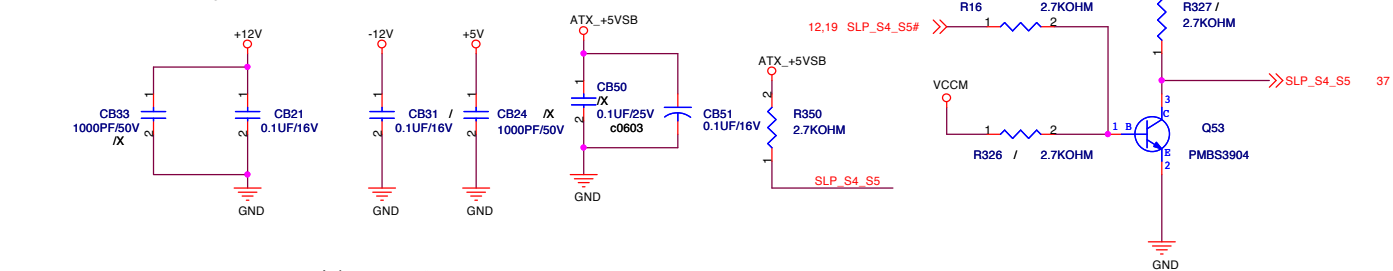
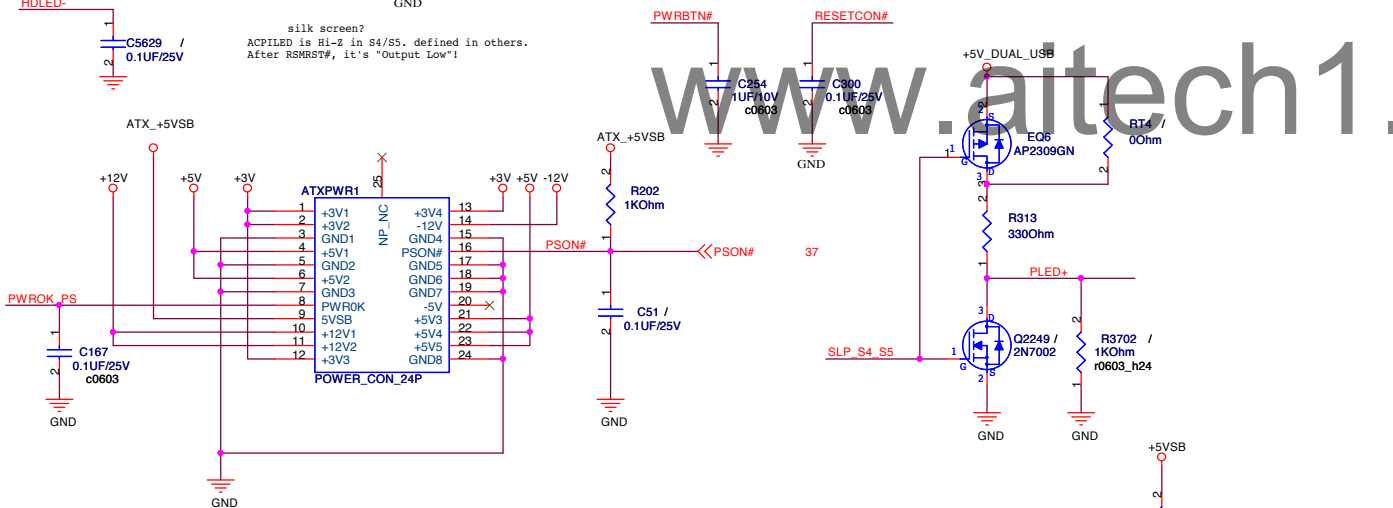
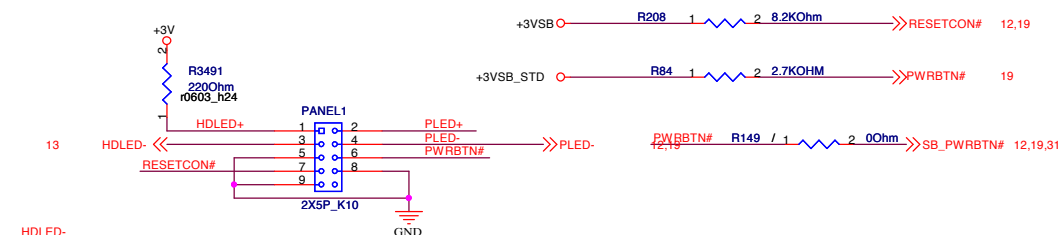
## Speak



**S3**

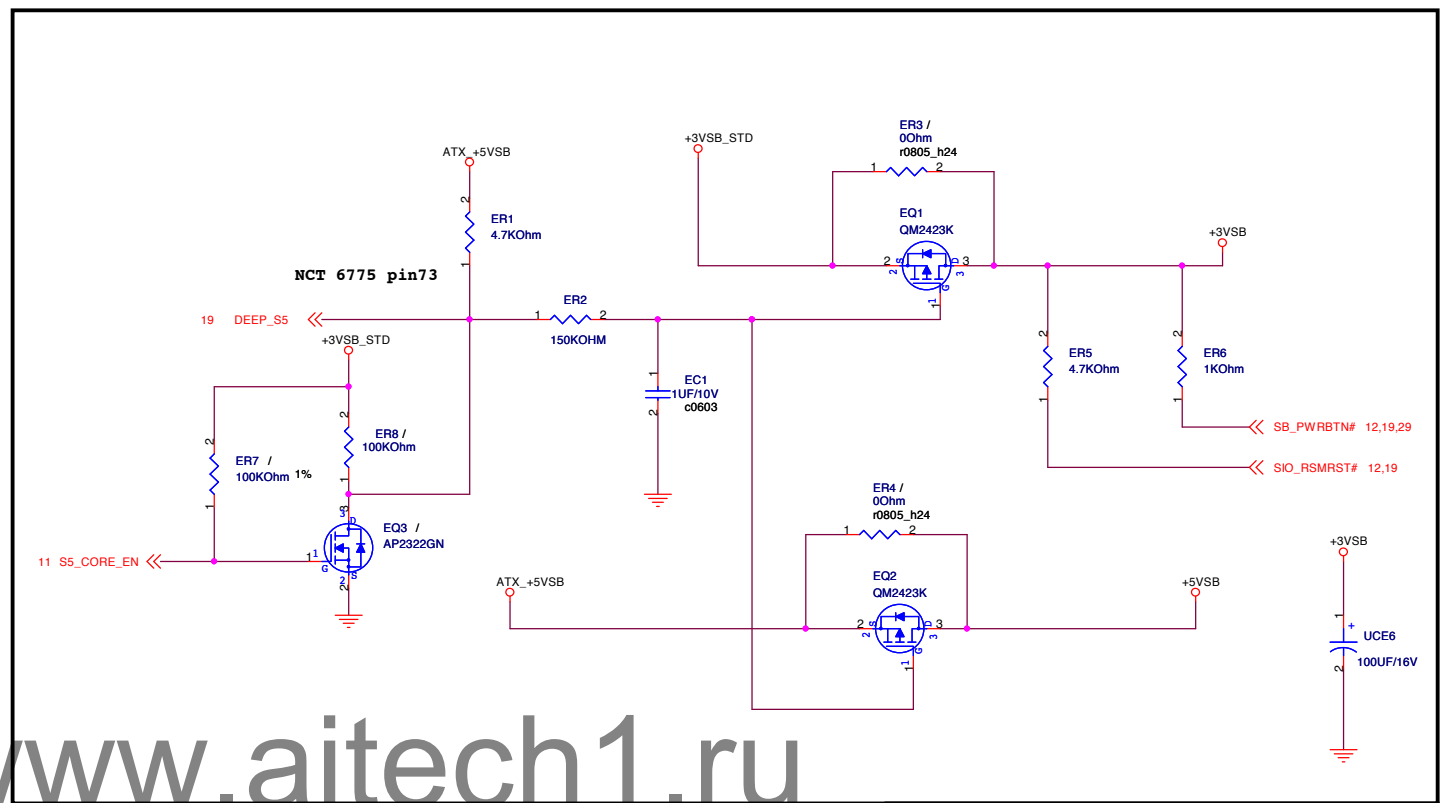


## FRONT PANEL

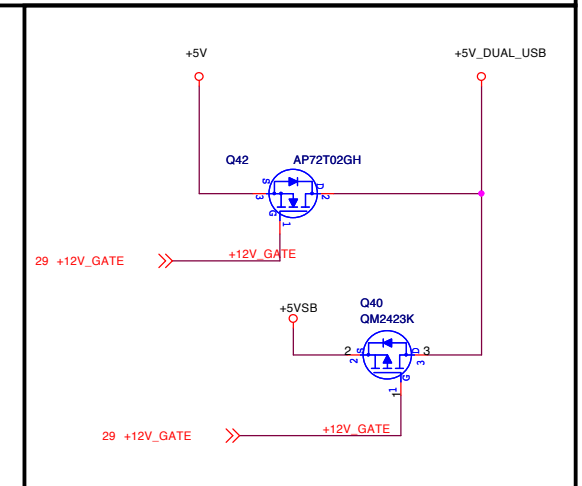
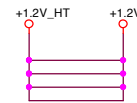


### Around the ATX Power Connector

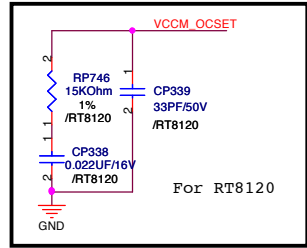




www.aitech1.ru

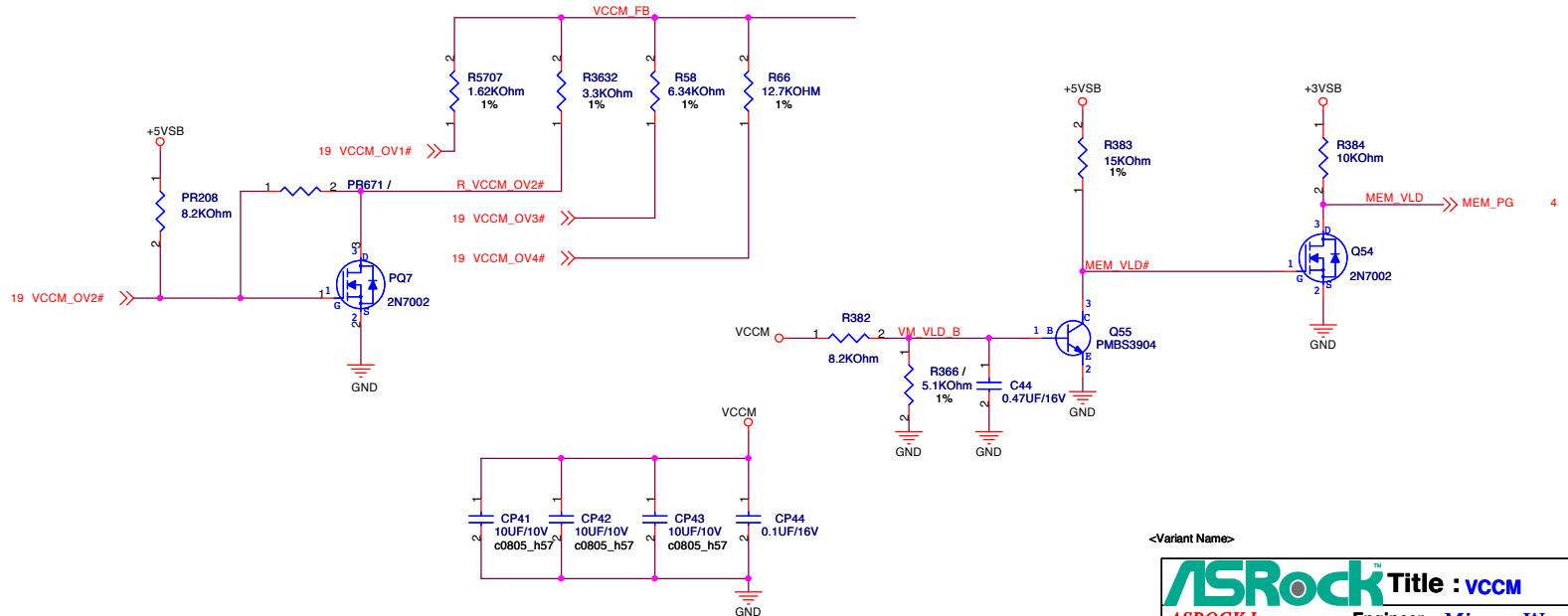


<Variant Name>



(Power-On default 1.5V )

OV4#	OV3#	OV2#	OV1#	Voltage
I	I	L	I	1.300
L	I	L	I	1.350
I	L	L	I	1.400
L	L	L	I	1.450
I	I	I	I	1.500
L	I	I	I	1.550
I	L	I	I	1.600
L	L	I	I	1.650
I	I	L	L	1.700
L	I	L	L	1.750
I	L	L	L	1.800
L	L	L	L	1.850
I	I	I	L	1.900
L	I	I	L	1.950
I	L	I	L	2.000
L	L	I	L	2.050

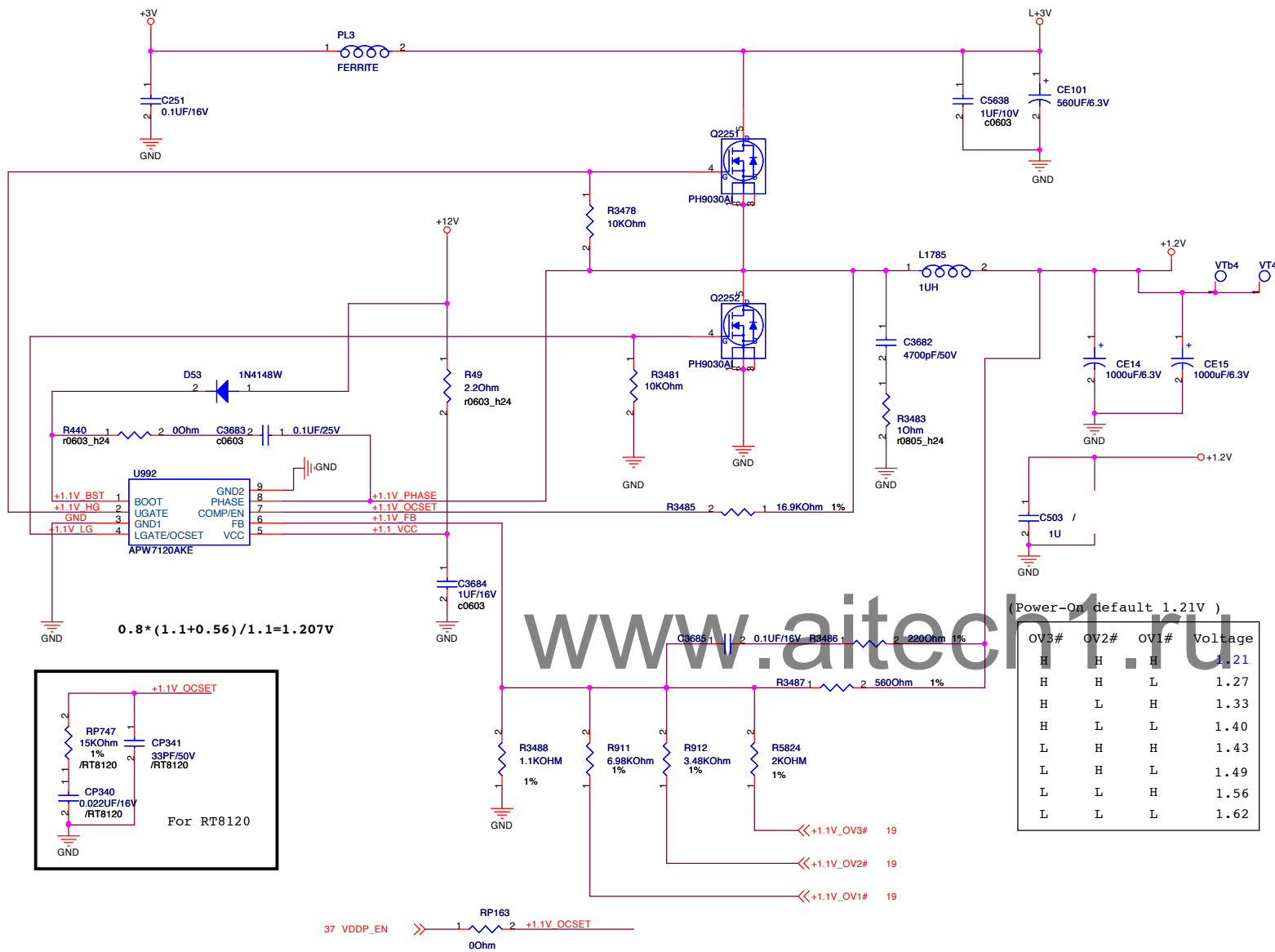


<Variant Name>

**ASRock** Title : **VCCM**

ASROCK Inc. Engineer: **Mingus Wu**

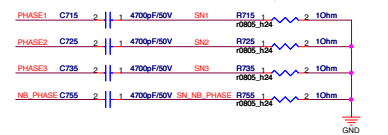
Size	Project Name	A55M-HVS	Rev 1.03
A3			
Date: Monday, April 02, 2012	Sheet 32 of 39		

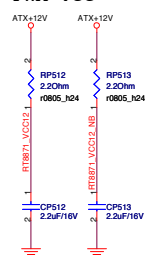


(Power-On default 1.21V )

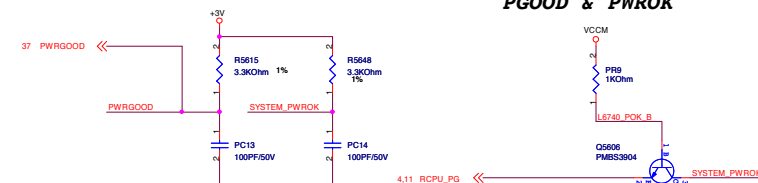
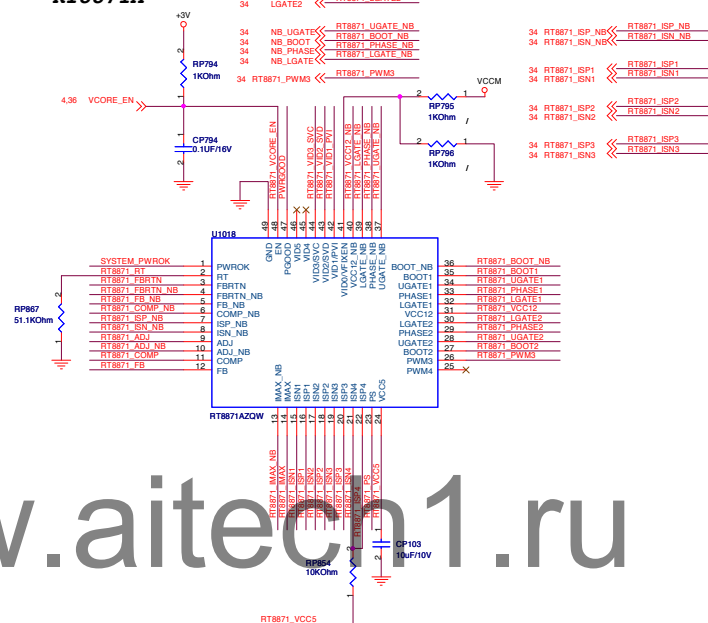
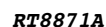
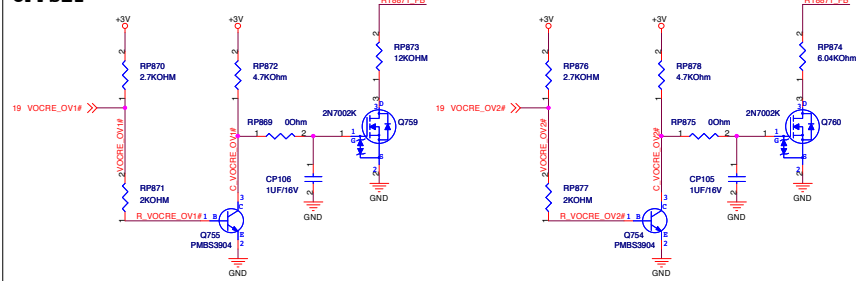
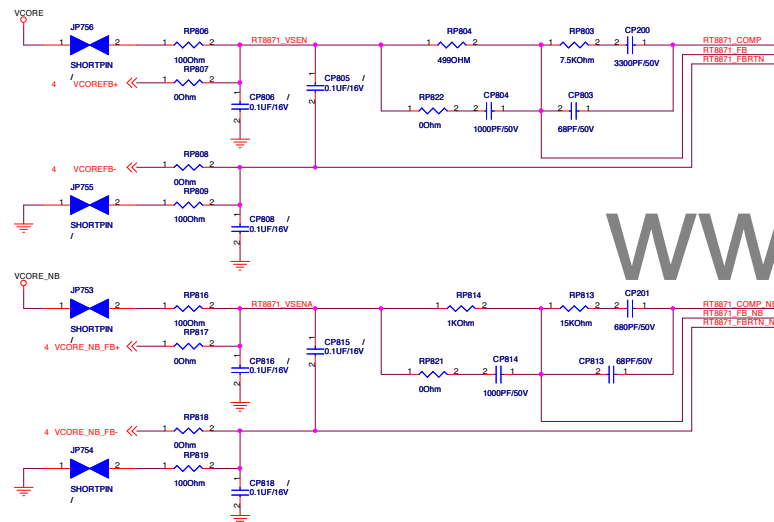
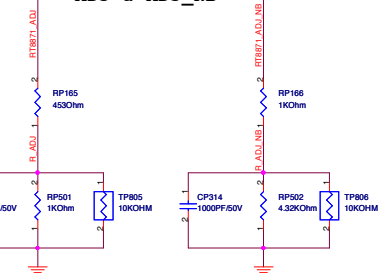
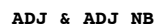
OV3#	OV2#	OV1#	Voltage
H	H	H	1.21
H	H	L	1.27
H	L	H	1.33
H	L	L	1.40
L	H	H	1.43
L	H	L	1.49
L	L	H	1.56
L	L	L	1.62

<Variant Name>

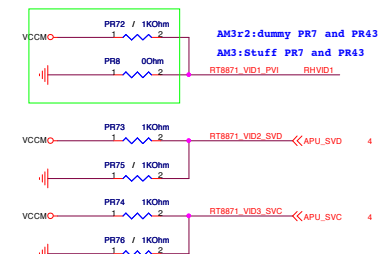




Close to RT8871

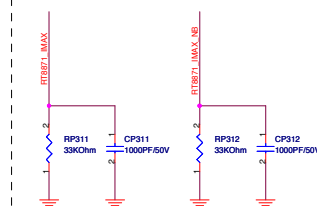


**VID**



www.aitech1.ru

## IMAX &amp; IMAX NB



&lt;Variant Name:

ASRock™ Title : VCore L6717

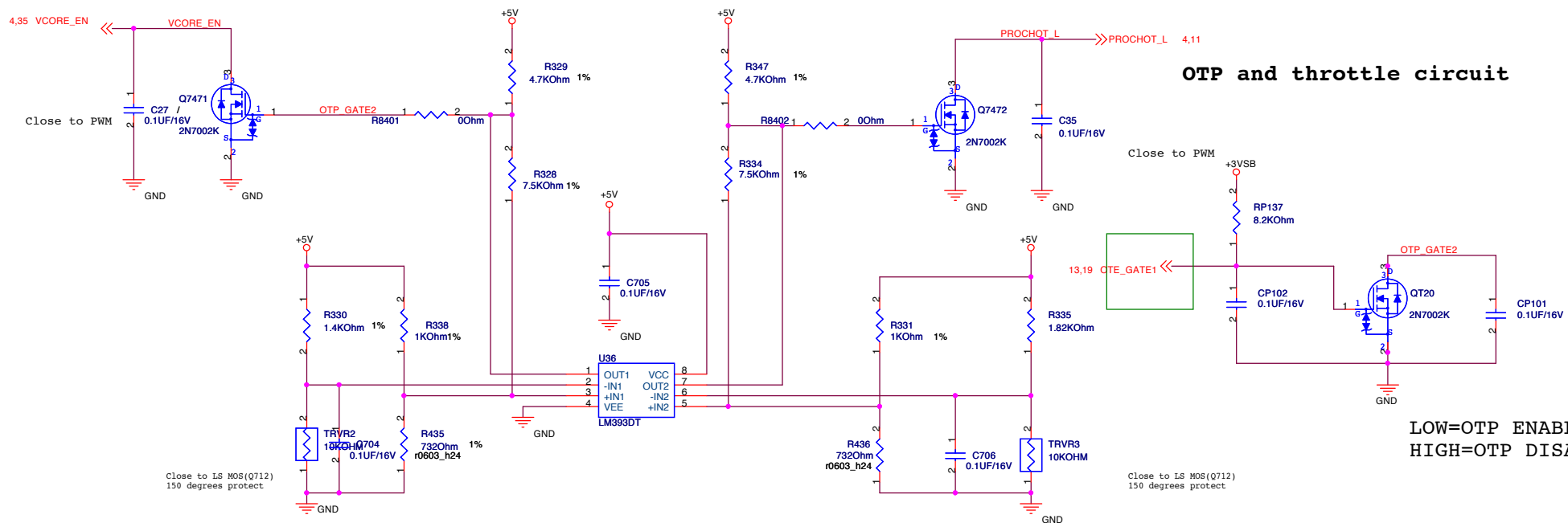
ASROCK Inc. Engineer: **Mingus Wu**

Size	Project Name
------	--------------

Size	Project Name
Custom	<b>A55M-HVS</b>

Date: Monday, April 02, 2012 Sheet 35 of

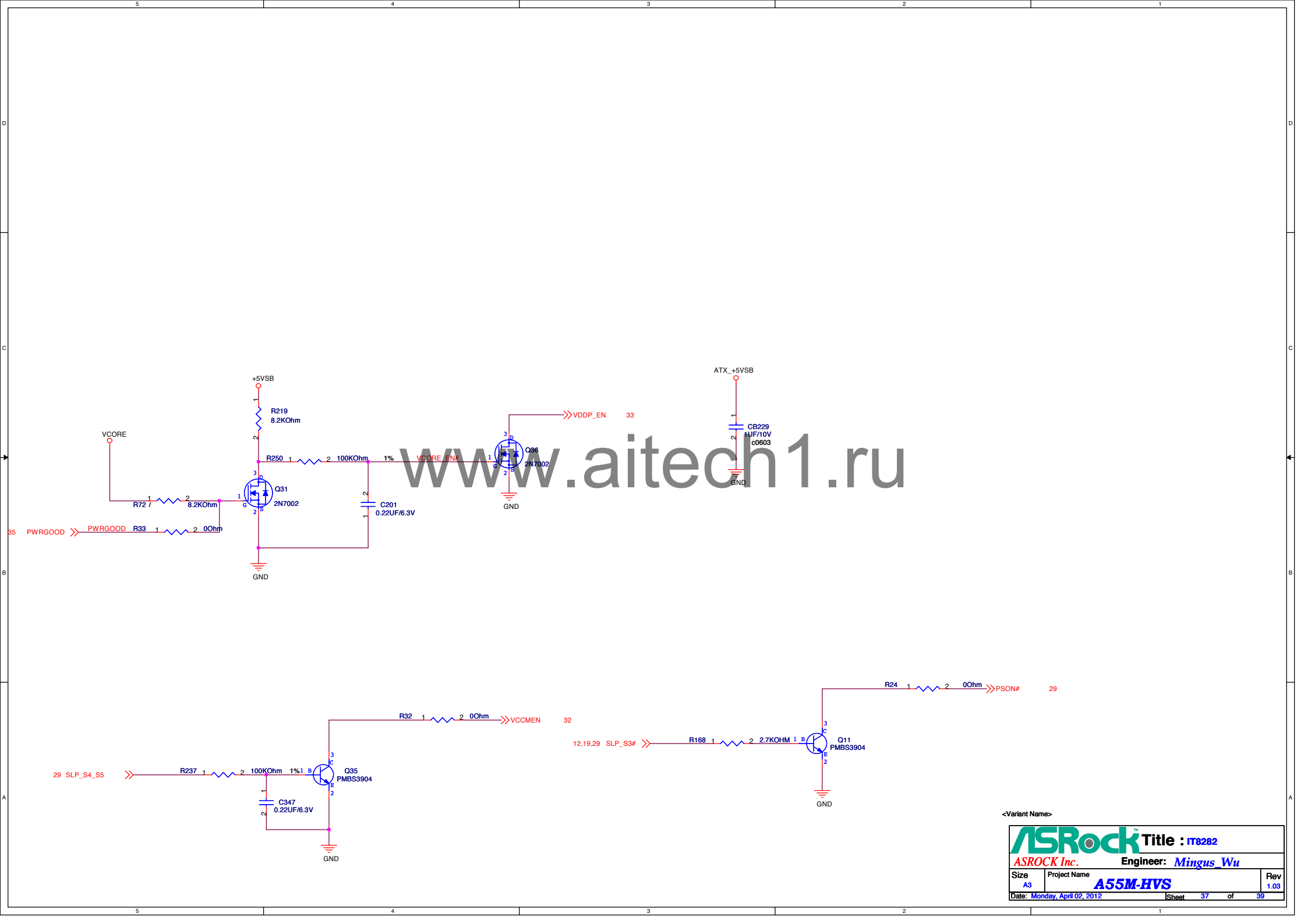
	Re
	1.4



www.aitech1.ru

<Variant Name>

<b>ASRock</b> ™		Title : <b>OTP</b>	
ASRock Inc.		Engineer: <b>Mingus Wu</b>	
Size A3	Project Name <b>A55M-HVS</b>	Rev 1.03	
Date: <b>Monday, April 02, 2012</b>		Sheet <b>36</b> of <b>39</b>	



4,11 APU\_RST#  
4 CPU\_DBREQ\_L  
4 CPU\_DBRDY  
4 CPU\_TCK  
4 CPU\_TMS  
4 CPU\_TDI  
4 CPU\_TRST\_L  
4 CPU\_TDO

T69 1 TPC26b

T70 1 TPC26b

VCCM

R5771 /X  
10KOhm

TPC26b 1 T71

www.aitech1.ru

TPC26b 1 T72

+3VSB

VCCM

R5781  
10KOhm

R5782  
10KOhm

OR38 00hm  
1 2

+3VSB

VCCM

R5787  
10KOhm

R5788  
10KOhm

OR37 00hm  
1 2

VCCM

+3VSB

R5789  
10KOhm

R5790  
10KOhm

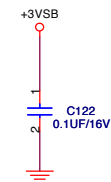
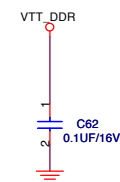
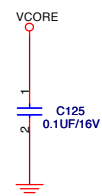
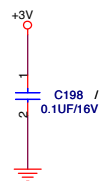
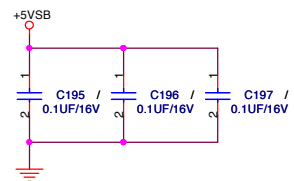
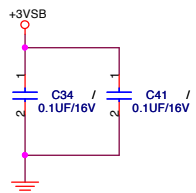
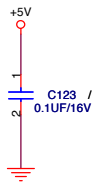
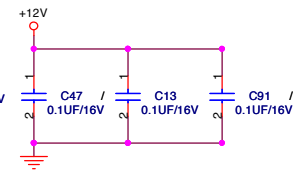
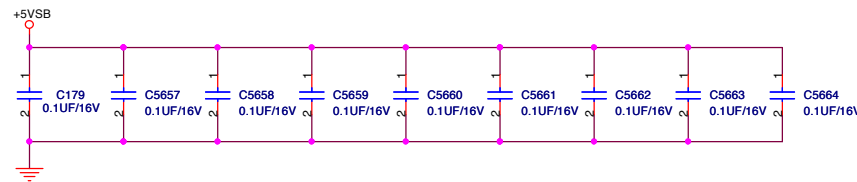
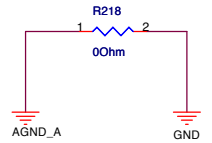
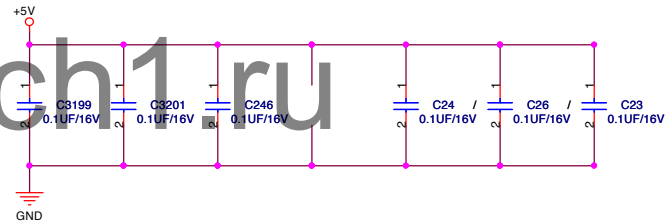
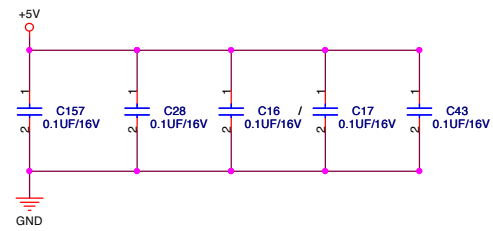
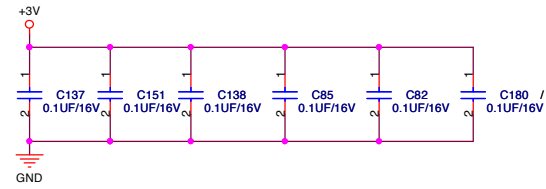
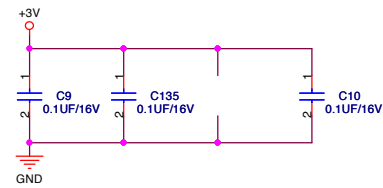
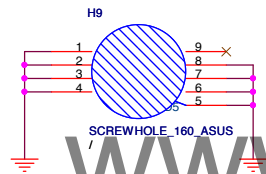
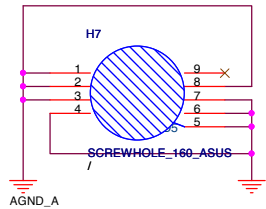
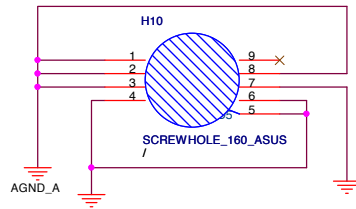
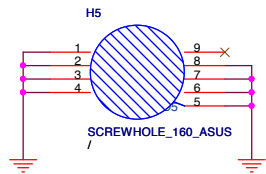
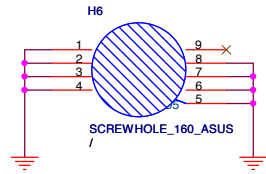
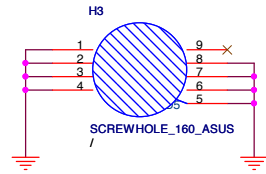
OR25 00hm  
1 2

IMC\_TCK 12

<Variant Name>

<b>ASRock</b> ™		Title : ACC & EUP & IOT	
ASROCK Inc.		Engineer: Mingus Wu	
Size A3	Project Name <b>A55M-HVS</b>	Rev 1.03	
Date: Monday, April 02, 2012		Sheet	38 of 39

# uATX scwew



<Variant Name>

ASRock		Title : SCREW	
ASRock Inc.		Engineer: Mingus Wu	
Size	Project Name	Rev	
A3	A55M-HVS	1.03	
Date: Monday, April 02, 2012	Sheet	39	of 39